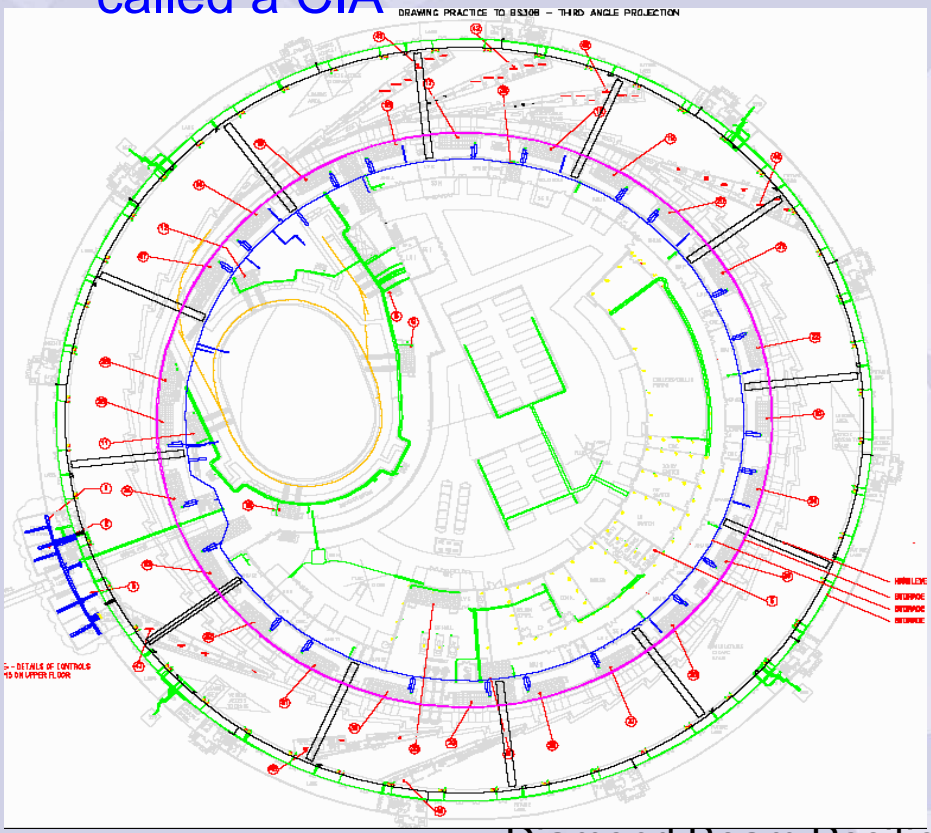
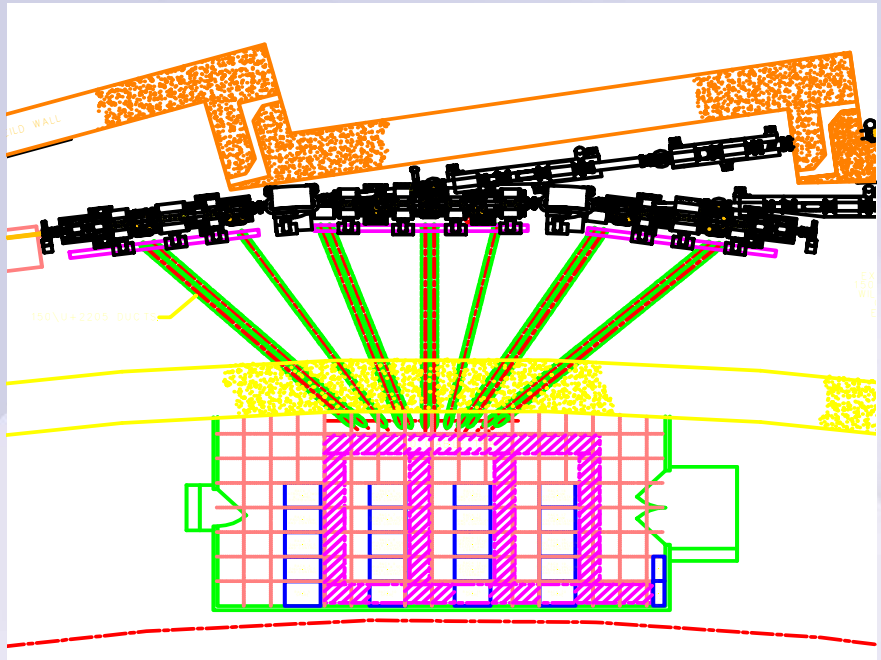
Diamond Beam Position Feedback

Structure of Diamond Storage Ring

- Storage Ring 24 Cells 560m circumference
- Each cell has control and instrumentation for that area in air conditioned, temp. stabilised room, called a CIA





- Each CIA houses the racks and instrumentation for that cell separate CS for each techical are PSUs, Vac, Diag,ID, FE etc
- Three Labyrinths through the shield wall to trenches in the SR tunnel

Cell Structure of Diamond Storage Ring

- Steering Magnets and Power supply rack (each cell)
  - PSU for 7x2 slow correctors in Sextupole magnets and 4 x 2 dedicated fast correctors
  - PSUs Interfaced with FO link to VME Crate
  - VME crate runs EPICS IOC, VME64x, VxWorks, Motorola MVME5500
  - Second VME processor board runs real time FB algorithm and receieving BPM data
- Electron Diagnostics rack (each cell)
  - 7 BPMs x 2 planes, Libera from Instrumentation Technologies
  - Virtex2Pro FPGA inside each BPM for digital down conversion and detection
  - 7 RocketIOs with SFP housings for fast communications
  - EPICS IOC, on Libera box, ARM processor, Linux
- Front End Photon Diagnostics (each cell)
  - 2 Front-ends per cell with 2 Photon monitors (pBPM) per Front-end
  - The current PBPMs monitored and controlled through analogue and serial
  - EPICS IOC, VME64x, VxWorks, Motorola MVME5500

Diamond SR Feedback Plan

- Day 1
  - Requires Slow Beam feedback to be available
  - Date determined by first beam in SR
    - Jan 2006
- Day 2
  - Requires Fast Beam feedback
  - 1 Year after day 1 !
- Why?
  - Initial work during 2006 will be to characterise the machine and will not need feedback
  - Feedback will possibly be required to correct for thermal drifts etc
  - We also need information for machine characterisation to complete dynamic analysis for fast FB design

Slow Beam Position Feedback

- Specified
  - Fs at 5 -10Hz, Closed loop BW of approx 0.5Hz
  - Realised over Channel Access
  - Data available from 168 SR eBPMs, 40 FE xBPMs and control of 336 Slow Correctors and 192 Fast Correctors
- Implementation
  - Dynamics of the system not significant as Fs low.
    - Effective apply repetitive corrections to orbit
  - Will be realised as Global (and Local loops if required)
- Progress
  - Tracy II model of SR implement under EPICS
    - Operational July 2004
  - MCA interface and MatLab name space implemented
  - Testing of MatLab based global FB against model planned for Sept 2004 when AP effort available

MatLab AT Based Feedback Application

Orbit Correct implemented using AT for Spear 3

Fast Beam Position Feedback

- Specified
  - Fs at 4kHz to 20 kHz, Closed loop BW >100Hz
  - Data transport to be realised over dedicated communication channel
  - Data available from 168 SR eBPMs, 40 FE xBPMs and control of 336 Slow Correctors and 192 Fast Correctors
  - Specification may change based on the characterisation of the SR
- Implementation
  - Dynamics of the system **ARE** significant
    - Require characterisation of SR
    - Require details of transfer characteristics of FB components
    - Use orbit correction algorithm (as per slow FB) but with controller and compensation filters
  - Will be realised on dedicated hardware for data distribution, and calculations

Data Transport

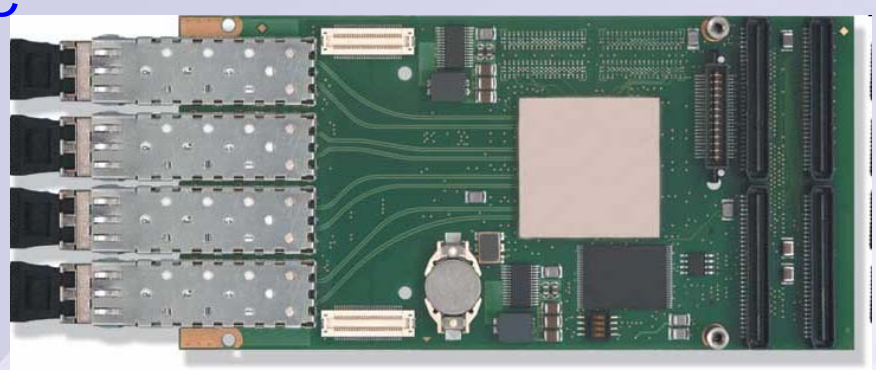
- Green Book (Diamond design) presented two schemes
  - Reflective Memory
    - Based on 49 RM VME boards, off the shelf but cost high
    - RM in every BPM and Steering VME crate
    - 49th board do data capture
  - Network Broadcast
    - Viable on small network (ALS), would have to characterise switches, and very dependent on 3RD party hardware
- Reconsidered transport based on selecting Libera eBPMS from Instrumentation Technology
  - Feedback working group considered two options
  - Network of Libera boxes Option 1 See Next slides
    - Data move (See Next slides)
    - Saves in cost of RM board
    - Gain network resilience
    - Need to develop VHDL components to realise data network
    - Still need to get data from Libera boxes into the VME crates
  - Reflective memory Option 2 See Next slides
    - Using 25 Reflective Memory PMC boards on feedback computation processor
    - 25th board do data capture
    - Cost of PMC RM boards is reduced cf to VME RM boards
    - Of the shelf solution
    - Still need to get data from Libera boxes into the VME crates

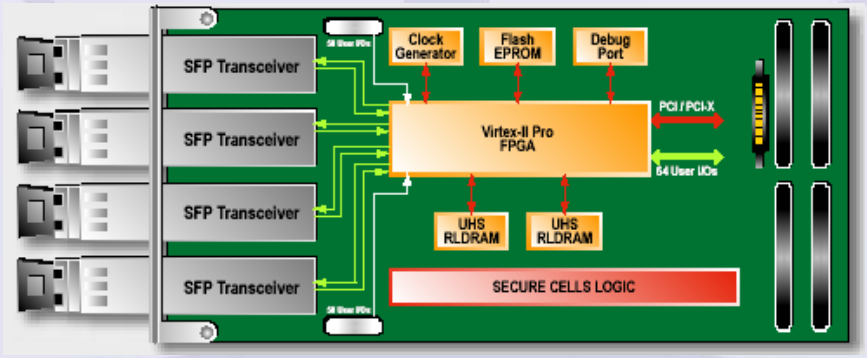
Hardware Interconnect One Cell

- Main processor provide CS control of PSUs and control of FB process via shared memory.
- Uses Event Network for synchronisation of BPMs and computation
- Uses second processor in PSU VME crate for FB calculations
  - Standard processor MVME5500, running VxWorks OS
  - Bench marked and is fast enough ie no DSP
- pBPM integrated using analogue signals
- eBPMs from Libera Boxes integrated using PMC module on second processor, with Rocket IO to SFP module and FO cable
- PSU interface using PSU IF as IP module on VME IP Carrier connection to PSU using 5 Mbit FO cables

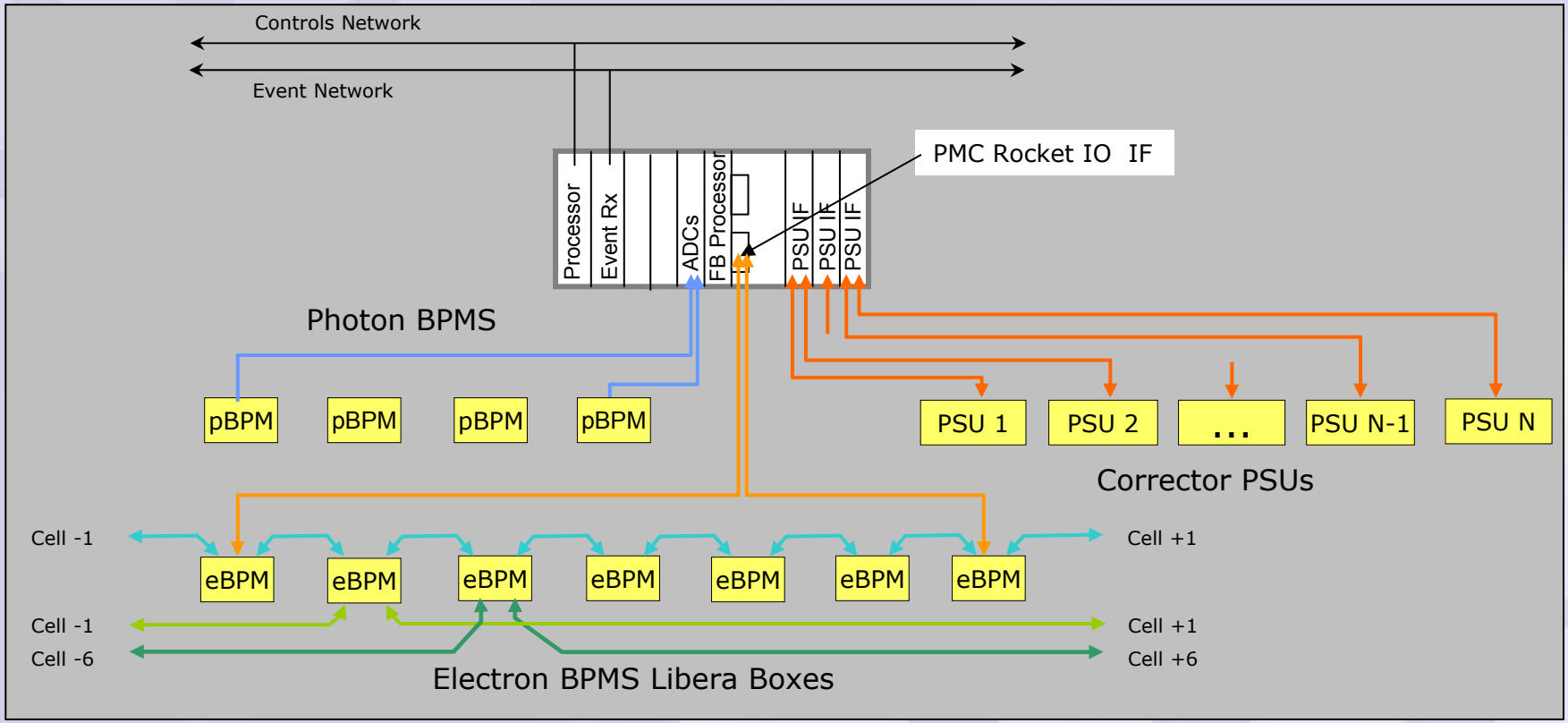
Libera Interface to VME Syetem

- Looking to use a commercial PMC module CES GPIO 8409
  - Virtex-II Pro FPGA
  - 4 SFP housings (optical or electrical transceivers possible)
  - Tools for VxWorks and for FW development
- Performance of data transfer from PMC to the main memory of the host carrier board, data block transfer time:
  - 7us = 168*20Bytes @ 500MB/s
  - 28us = 168*20Bytes @120MB/s





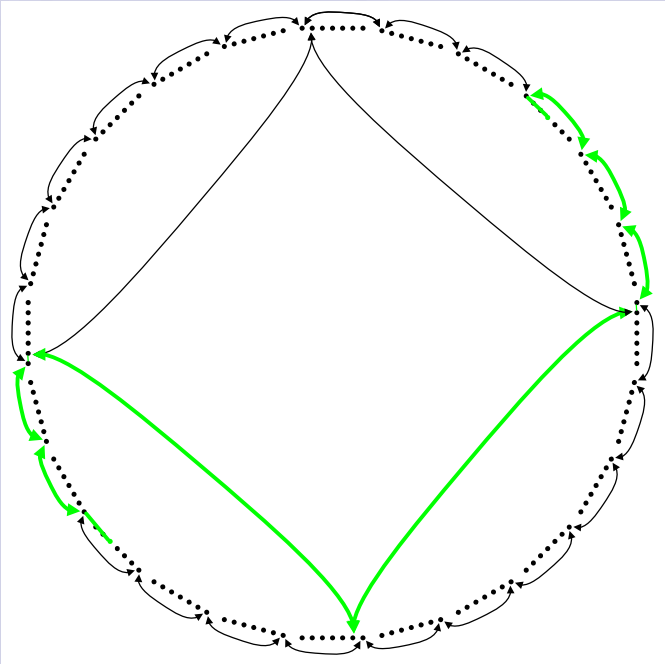
Option 1 Libera Network One Cell



- Uses interconnect of Libera boxes to move all BPM data to all cells
- Libera boxes interconnected in a redundant ring
- xBPM data ether written to Libera unit from VME or on simulated Libera units with ADCs

Option 1 Libera Network Structure

- Forms ring with bidirectional neighbour to neighbour links for each BPM
  - 1-cell bypass ring overlay of 24 links
  - 6-cell bypass ring overlay 4 links
  - All three rings are independent
  - Trade off between latency, wiring effort and wiring complexity
  - Redundant for at least one link or BPM failure per cell



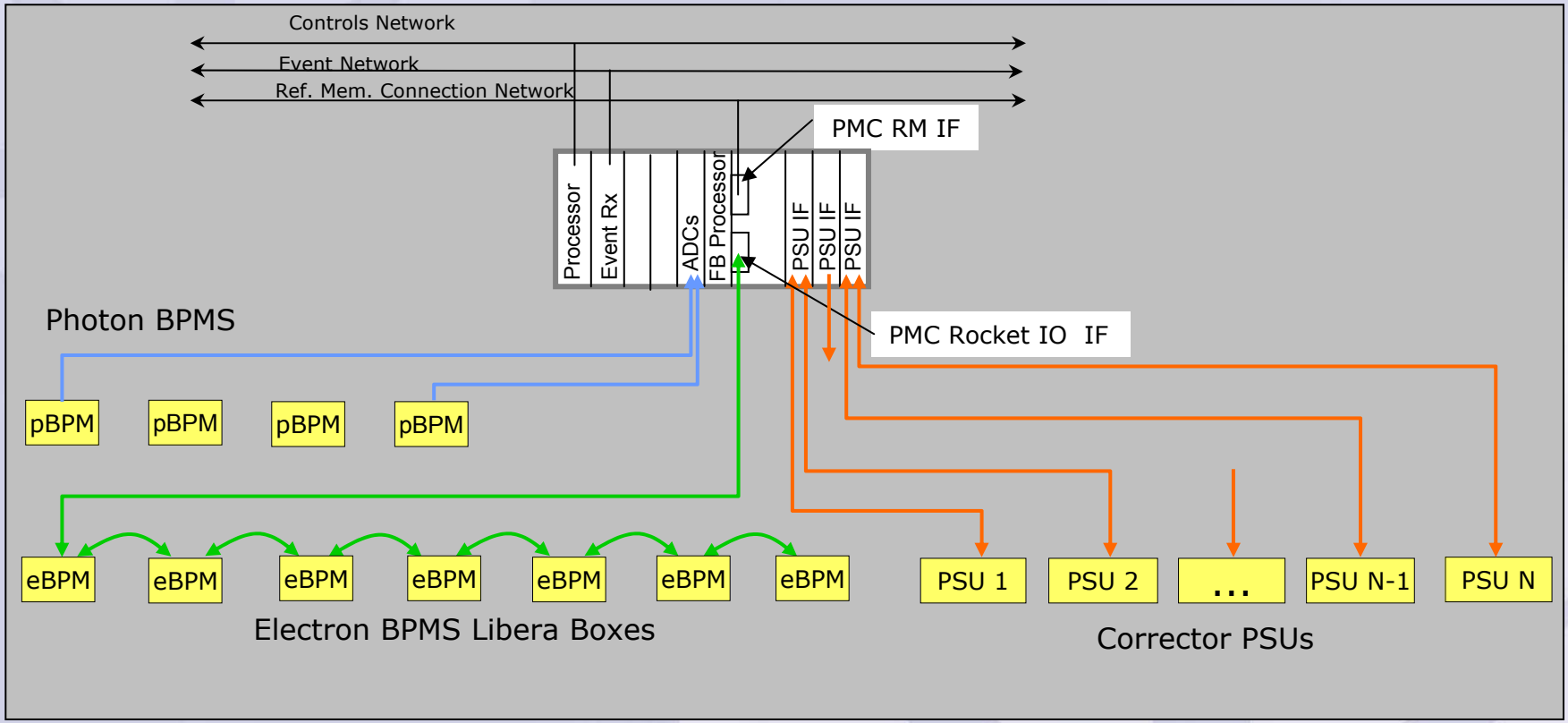
- Normally for data to get from one BPM to all others
  - max hop count of a packet: 3+3+1+2+1+2+3 = 15
  - max hop count of a packet one node faulty: 3+12+3 = 18
  - max hop count of a double fault nodes faulty: 5+5+1+2+1+5+6 = 25
- Propagation time ~ 1usec per hop

  Better than 25usec

Option 1 Libera Network Realisation

- The functional interconnection of the Libera boxes is not part of the BPM contract
  - The Libera boxes use Xilinx FPGA with high speed serial interconnects Rocket IO
  - The contract does include the hardware to make these interconnects available to SFP module, allow use of SM or MM Fibre
- The PMC to Rocket IO module is off the shelf
- DLS has contract with Super Computing Systems to specify the functionality to interconnect the BPM boxes and move the data into the VME system
  - VHDL components.
  - This specification can then be used either to do the work in-house (FPGA engineer) starts in Oct 2004 or to put out to industry
    - SCS and I-Tech would potentially be interested and have the necessary skills.

Option 2 Reflective Memory Network One Cell



- Uses interconnect of VME crate using PMC Reflective Memory modules to move all BPM data to all cells
- Libera boxes connected to PMC module in VME second Processor

Option 2 Reflective Memory Network

- VMIPMC-5565 Fiber-Optic PMC Reflective Memory
- Data rate 2.12 GBaud serially
- Data written to memory in one node is also written to memory in all nodes on
- the network
- 25 nodes
- Connection single-mode fiber
- Dynamic packet size, 4 to 64 bytes of data
- Transfer rate 43 MByte/s (4 byte packets) to 174 Mbyte/s (64 byte packets)
- Star Configuration with Reflective Memory Hub Assembly

Feedback Software

- Each Steering Crate calculates new PSU values for 22 PSUs from all eBPMs and pBPMs
  - Performance on MVME5500 11 to 22usec, Non optimised
- Calculation will include Logic to select BPMs, multiplication of a sub matrix of Inverse Response Matrix, controller and filters
- Control and monitor of FB calculation, setting of coefficients etc through EPICS using shared memory into 2nd processor
- Second processor run VxWorks but no EPICS and no network stack

Photon BPMs

- Electrical and control system design for each Front End includes provision for 2 pBPMs
- Phase 1 Front Ends I06 and I18 will have photon monitors installed on day 1
  - Selected pBPMS from Feinwerk- und Meßtechnik GmbH FMB
- For FMB pBPMs
  - Control will be provided for Stepper motor to align and for control of bias and amplifiers over RS232
  - Analogue position outputs will go into ADCs in Front End control system
    - This is suffice for slow FB over channel access.
    - When required for fast FB the signal will be electrically copied or moved into ADCs in fast FB system
- Cabling and infrastructure for pBPMs for all Phase 1 Front Ends is included in initial installation and space in Front end design

Fast FB Progress

- Detail design and implementation is planned for 2006-2007
- Progress in terms of preparation work during 2004-2005
  - BPMs
    - Need to develop an model of Libera box 2005 onward
  - Vessel
    - Need to be characterised, may use beam hence 2006 on
  - Data Distribution
    - Fibres included in network contract
  - Magnet
    - H(S) should be measure
  - PSU
    - Characterise PSUs for Steerer, PSU for Fast corrector being designed
    - Simulink model of PSU and controller
    - Measured communication delay from VME crate, need to include in PSU model
  - Computation
    - Building libraries and bench marking performance on MVME5500 August 2004
  - Data Transport
    - Supercomputing Systems working on network structures
    - Develop VHDL modules for Libera Boxes and VME PMC module
    - Either Contract or In-house

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